ROHDE&SCHWARZ
BROADCASTING DIVISION

Digital TV
Rigs and Recipes
Part 5
ITU-T J.83/B

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Contents

5. Introduction

For optimal transmission, data not only has to be coded to MPEG2 (Motion Picture Experts Group), which reduces the data rate of the ITU-R BT.601 interface from 270 Mbit/s to typically 3 to 5 Mbit/s, but also subjected to a special type of modulation (see "Digital TV Rigs and Recipes" – Part 1 "ITU-R BT.601/656 and MPEG2"). Same as for the DVB standards, a comparison of analog modulation with digital modulation as used by the North American ITU-T J.83/B cable standard reveals that digital modulation yields a flat spectrum with a constant average power density across the 6 MHz channel bandwidth. The modulator (and, consequently, the demodulator) employed by the ITU-T J.83/B standard is of more complex design than the DVB-C modulator commonly used in Europe and many other countries. Using concatenated coding for the MPEG2 data, ITU-T J.83/B offers forward error correction better than that of DVB-C.

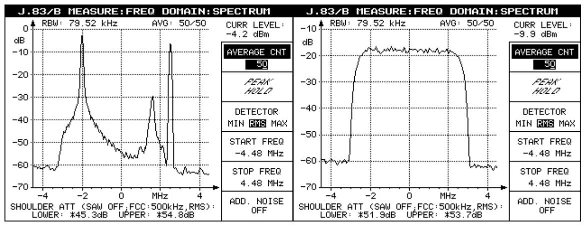

Fig. 5.1 Comparison of M/NTSC spectrum and ITU-T J.83/B spectrum

5.1 Modulation to ITU-T J.83/B (North American Cable Standard)

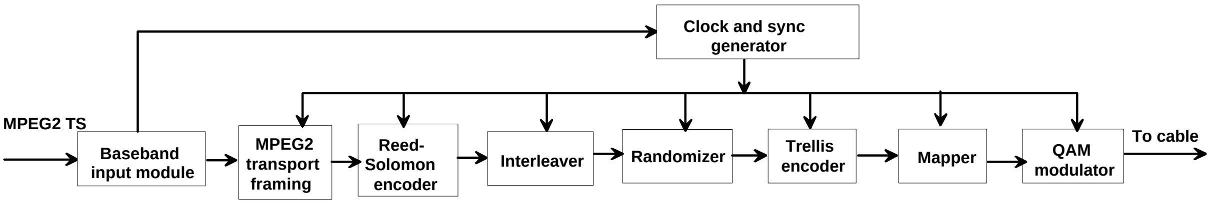

Fig. 5.2 Block diagram of ITU-T J.83/B modulator/converter

5.1.1 Baseband Input Module

The MPEG2 transport stream (TS) packets are routed to the first function block of the digital TV modulator, which is the baseband input module, via one of the following interfaces:

SPI (synchronous parallel interface)
ASI (asynchronous serial interface)
SSI (synchronous serial interface)
SDTI (serial digital transport interface)
HDB3 (high density bipolar of order 3)
ATM (asynchronous transfer mode)

The TS packets are transported to the baseband input module at the specified ITU-T J.83/B data rates of 26.97035 Mbit/s net for 64QAM and 38.81070 Mbit/s net for 256QAM. The standard does not provide for other QAM modes. The baseband input module reconstructs the original TS data, optimizes return loss, and corrects amplitude and phase response versus frequency. It supplies all the required information to the clock and sync generator function block, which acts as a central clock generator for all other function blocks of the ITU-T J.83/B modulator. This information includes, for example, the data rate, which is derived from the incoming TS data, and in the case of the SPI interface, also sync byte signalling for the TS packet and data valid signalling via the data valid line. The reconstructed TS packets are taken from the baseband input module to the next function block, i.e. MPEG2 transport framing.

5.1.2 MPEG2 Transport Framing

After the input module, the TS packets undergo the first processing step:
To ensure reliable synchronization at the receiver end and to provide additional error correction capability, the MPEG2 transport packet structure is modified by substituting a parity checksum for the 0x47 sync byte which, in line with MPEG2, is the first byte of each TS packet. The parity checksum byte is obtained by means of sliding computation, then the sync byte is deleted, and the parity checksum byte appended at the end of the remaining 187 bytes of the TS packet. In this way, a 188-byte packet is obtained again.

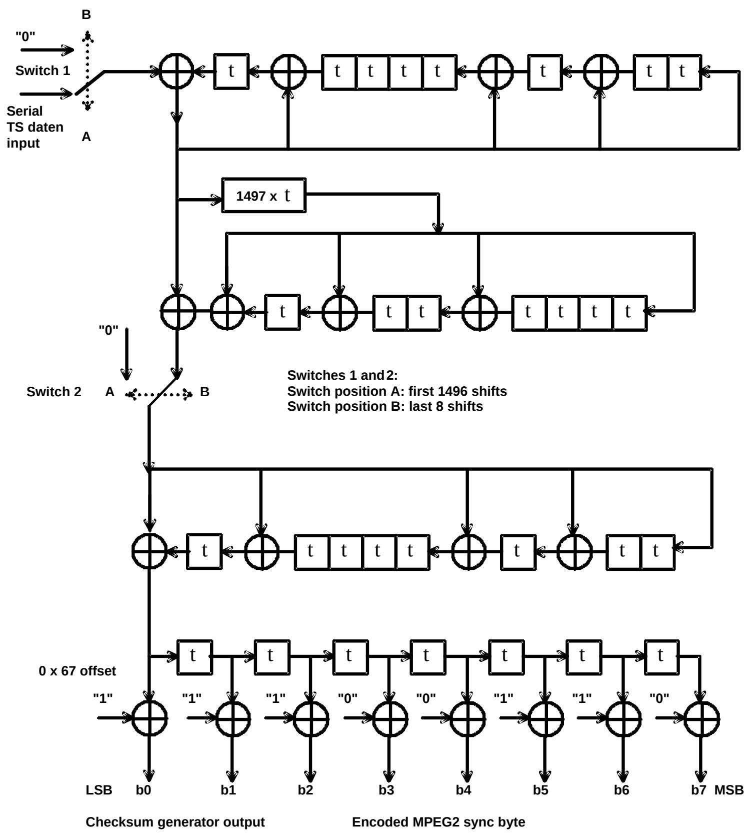

Fig. 5.3 Checksum generator for MPEG2 sync byte encoding

MPEG2 data is applied as serial data to the input of the checksum generator. This means that TS packets with a length of $188 * 8 = 1504$ bits are present. Checksum computation covers only 187 bytes however, so that the actual data volume is 1504 – 8 = 1496 bits.
The checksum generator is described by the following equation:

$$f(x) = \frac{1 + x^{1497} * b(x)}{g(x)} \quad \text{where}$$

$g(x) = 1 + x + x^5 + x^6 + x^8$ and
$b(x) = 1 + x + x^3 + x^7$

Prior to the start of the encoding operation, all clock buffers are set to zero. Then the 1496 bits are shifted into a feedback shift register. After the 1496 clock bits, the shift register is also set to zero by means of equation g(x). Using the last eight clock bits with the offset 0x67, the checksum, i.e. the coded sync byte, is generated. This sync byte, in turn, produces the original 0x47 sync byte at the decoder end. The syndrome generator employed for this purpose is illustrated below:

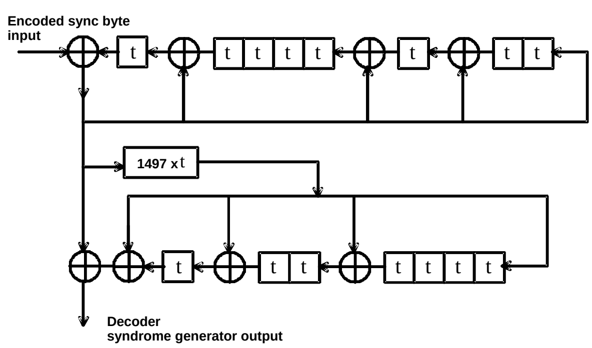

Fig. 5.4 Syndrome generator for MPEG2 sync byte decoding

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If a valid code word is present at the syndrome generator input, the original 0x47 sync byte is restored at the generator output, i.e. the code word is replaced by the valid sync byte. In this way, a standard TS packet of 188 bytes length with the sync byte as the start byte is reproduced. It should be noted, however, that the sync byte is derived from the preceding TS packet and not from the 187 bytes following the sync byte.

Instead of the syndrome generator, a matrix operation can be employed at the decoder end to check whether a valid code word is present.
In this case, a vector R of 187 bytes of MPEG2 data and the checksum byte are applied to the decoder. Vector R has a size of 1 x 1504 (each TS packet contains 8 x 188 = 1504 bits). The vector is modulo 2 multiplied with a parity check matrix P of the size 1504 x 8. If data has been transmitted error-free, this operation yields a vector S of the size 1 x 8 and with the contents S = [0100 0111] = 0 x 47, which is the original sync byte of the TS packet.

For the parity check matrix P, a vector C of a size of 1 x 1497 has to be defined first. Vector C is structured as follows:

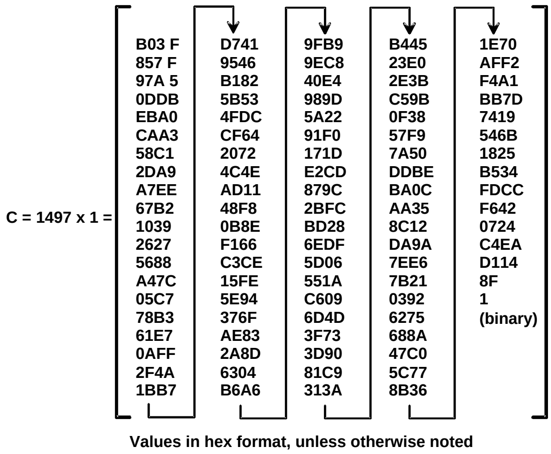

Fig. 5.5 Vector C

The hex values are entered serially bit by bit into the vector column, yielding a column length of 1497 bits.

Vector C is duplicated to produce the matrix P according to the following scheme:

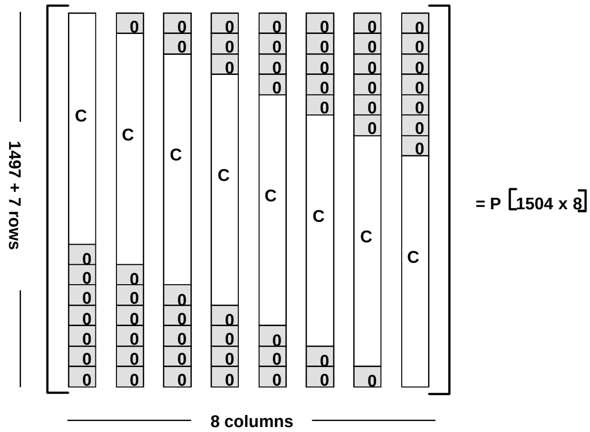

Fig. 5.6 Parity check matrix P

Vector C is extended by seven zero bits and duplicated into seven more columns, each column shifted down by one bit position relative to the previous column. In this way, the eight-column matrix P is obtained.
The matrix is modulo 2 multiplied with the received vector R to yield the original 0x47 sync byte.

5.1.3 Reed-Solomon (RS) Forward Error Correction (FEC)

The output of the checksum generator is applied to the input of the Reed-Solomon encoder block. In a first step for RS encoding, the TS packet data is divided into sections of 7 bits referred to as symbols. Of these 7-bit symbols, RS blocks are formed, each block consisting of 122 symbols plus six 6 appended RS FEC symbols. The resulting t = 3, (128, 122) RS FEC code is capable of correcting up to three errored symbols per block. This means that a quasi-error-free (QEF) data stream with approximately one uncorrected error event every 15 minutes will be obtained, assuming a BER of 7×10^{-5} or better before RS FEC (BER value determined empirically).

ITU-T J.83/B defines different FEC frame formats for the two modulation modes used, i.e. 64QAM and 256QAM.

5.1.3.1 FEC Frame Format for 64QAM

For 64QAM, an FEC frame is formed by 60 RS blocks, each containing 128 symbols, to which a frame sync trailer consisting of six 7-bit symbols is appended.

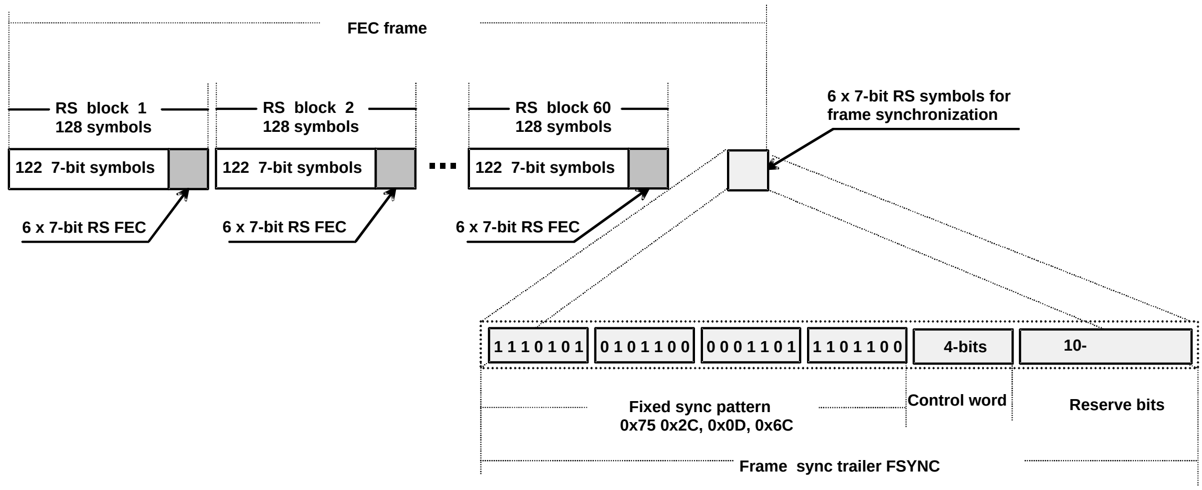

Fig. 5.7 FEC frame format for 64QAM

The frame sync word (FSYNC) consists of a fixed synchronization pattern of four 7-bit RS symbols (111 0101, 010 1100, 000 1101, 110 1100), followed by a 4-bit control word and 10 reserved bits that are set to zero.
The control word indicates the interleaving level and the interleaving mode. The meaning of the four bits is explained in Table 5.2.

5.1.3.2 FEC Frame for 256QAM

For 256QAM, an FEC frame is formed by 88 RS blocks, each containing 128 symbols, to which a frame sync trailer of 40 bits is appended.

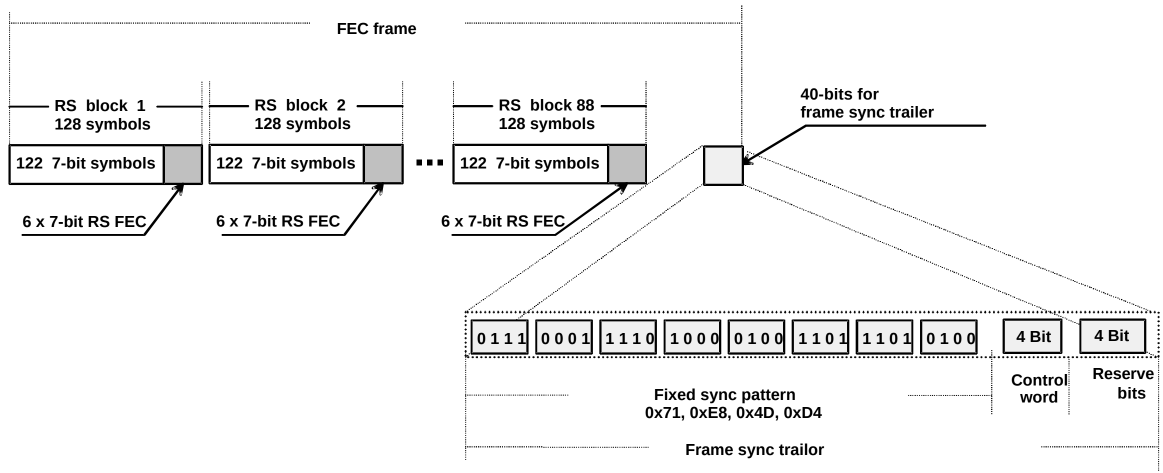

Fig. 5.8 FEC frame format for 256QAM

The frame sync trailer consists of a fixed synchronization pattern of four bytes (0x71, 0xE8, 0x4D, 0xD4), followed by a 4-bit control word and four reserved bits that are set to zero.

The control word indicates the interleaving level and the interleaving mode. The meaning of the four bits is explained in Table 5.2.

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5.1.4 Interleaver

Transmission errors usually corrupt not only a single bit but many bits following it in the data stream. Consequently the designation "error burst", which may comprise up to several hundred bits. The bits may even be deleted. The RS decoder correction capability of three symbols per RS block is insufficient in such cases. So an interleaver is used to insert – in the reduced interleaving mode – 8, 16, 32, 64 or 128 RS symbols (for the I = 8, 16, 32, 64 and 128 interleaver paths defined for the convolutional interleaver modes, see Fig. 5.9) from other RS blocks between neighbouring symbols of an RS block. This allows burst errors of max.

3 x 8	=	24	RS symbols
3 x 16	=	48	RS symbols
3 x 32	=	96	RS symbols
3 x 64	=	192	RS symbols
3 x128	=	384	RS symbols

to be corrected, provided that only three or fewer errored symbols per RS block occur after the deinterleaver in the receiver/decoder.

The enhanced interleaving mode provides for I = 128 paths with different memory depths of M = 1 to 8.

Reduced interleaving mode	
Paths	I = 8, 16, 32, 64, 128
Interleaving depth of FIFOs	M = 1, 2, 4, 8, 16
Enhanced interleaving mode	
Paths	I = 128
Interleaving depth of FIFOs	M = 1 to 8
Synchronization	At beginning of FEC frame via first path

Table 5.1 Level 2 interleaving

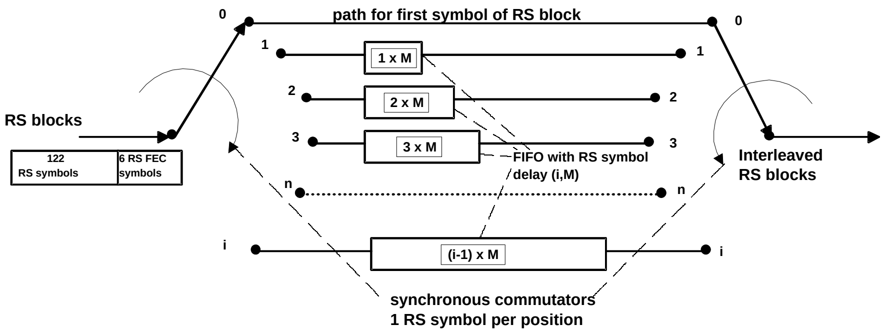

Fig. 5.9 Convolutional interleaver

The interleaving mode used (see Table 5.1) is indicated by the 4-bit control word of the frame sync trailer. Table 5.2 shows the interleaving level and the meaning of the control word in each case.

Depending on the interleaver configuration, level 1 (64QAM only) or level 2 (64QAM and 256QAM) interleaving capability is available.

Level 1 interleaving for 64QAM						
Control word (4 bits)	Paths (I)	Interleaving depth (M)	Max. length T_{Error} (µs) of an error burst		Latency T_L (ms) of interleaver	
			64QAM	256QAM	64QAM	256QAM
XXXX	128	1	94.92	65.98	4.018	
Level 2 interleaving for 64QAM and 256QAM						
Control word (4 bits)	Paths (I)	Interleaving depth (M)	Max. length T_{Error} (µs) of an error burst		Latency T_L (ms) of interleaver	
			64QAM	256QAM	64QAM	256QAM
0001	128	1	94.92	65.98	4.018	2.793
0011	64	2	47.46	32.99	1.993	1.386
0101	32	4	23.73	16.49	0.981	0.682
0111	16	8	11.86	8.25	0.475	0.330
1001	8	16	5.93	4.12	0.221	0.154
1011	Reserved					
1101						
1111						
0000	128	1	94.92	65.98	4.018	2.793
0010	128	2	189.8	132.0	8.036	5.586
0100	128	3	284.8	197.9	12.06	8.379
0110	128	4	379.7	263.9	16.07	11.17
1000	128	5	474.6	329.9	20.09	13.97
1010	128	6	569.5	395.9	24.11	16.76
1100	128	7	664.4	461.9	28.13	19.55
1110	128	8	759.4	527.8	32.15	22.35

Table 5.2 Interleaving levels and control words

5.1.5 Randomizer

The randomizer provides for even distribution of the 7-bit RS symbols in the constellation diagram. This ensures constant power density across the ITU-T J.83/B spectrum and allows the demodulator to maintain stable synchronization.

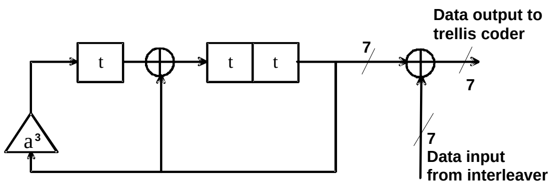

Fig. 5.10 Randomizer

The randomizer adds a PRBS over a Galois field(128) polynomial defined as follows:

$f(x) = x^3 + x + \alpha^3$
where $\alpha^7 + \alpha^3 + 1 = 0$

The resulting combinations are 7 bits wide, each constituting exactly one RS symbol.

For synchronization, the three buffers of the randomizer are reset to zero during the synchronization bits of the frame sync trailer at the end of the RS FEC frame (see 5.1.3 "Reed-Solomon (RS) Forward Error Correction (FEC)"). The randomizer is enabled at the first RS symbol of the RS FEC frame, i.e. after the trailer, and disabled after the last RS symbol of the last RS block of the FEC frame. Thus the synchronization bits are not randomized.

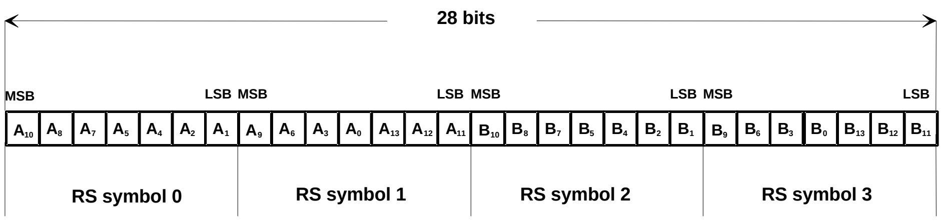

Fig. 5.11. 'A' and 'B' symbols for 64QAM

5.1.6 Mapping of Randomized Data to 64QAM and 256QAM Symbols

So far, we have discussed only bits and RS symbols. To transmit this data using 64QAM/256QAM (quadrature amplitude modulation), it has to be converted to QAM symbols. As a first step to this effect, trellis groups are formed from the randomizer output data.

5.1.6.1 Mapping of Randomized Data to 64QAM Symbols

With 64QAM, a trellis group consists of 28 bits, i.e. four randomized RS symbols. The bits of the four symbols are resorted and organized in 'A' symbols and 'B' symbols as shown in Fig. 5.11.

The trellis group thus obtained is applied to the input of the 64QAM trellis coded modulator. In the input block of the 64QAM modulator, the 'A' and 'B' symbols are resorted a second time and the four MSBs and the two LSBs for the QAM mapper are generated. The four MSBs are input to the mapper uncoded, the two LSBs undergo differential encoding.

The data has the following structure:

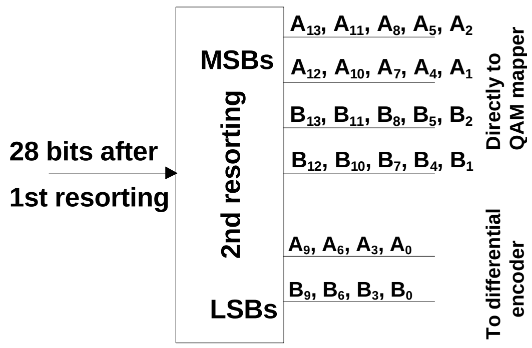

Fig. 5.12 Second resorting of 'A' and 'B' symbols of a trellis group

Tabular representation of trellis group symbols after second resorting:

	64QAM symbols				
	T_0	T_1	T_2	T_3	T_4
Directly to mapper	B_2	B_5	B_8	B_{11}	B_{13}
	B_1	B_4	B_7	B_{10}	B_{12}
	A_2	A_5	A_8	A_{11}	A_{13}
	A_1	A_4	A_7	A_{10}	A_{12}
To diff. encoder	B_0	B_3	B_6	B_9	
	A_0	A_3	A_6	A_9	
Time →					

Table 5.3 64QAM symbols of a trellis group

Table 5.3 shows that symbol T_4 has only four bits. The remaining two bits are generated by the trellis encoder and subsequent puncturing.
The above table also shows that the data of a trellis group corresponds to the five 6-bit 64QAM symbols T_0, T_1, T_2, T_3 and T_4.

Before being applied to the trellis encoder, the two LSBs undergo differential encoding, which considerably enhances decoding reliability of the ITU-T J.83/B receiver.

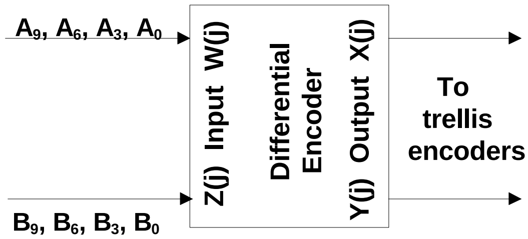

Fig. 5.13 Differential encoder

Differential encoding is based on the following equations:

$X(j) = W(j) + X(j-1) + Z(j)(X(j-1) + Y(j-1))$ and
$Y(j) = Z(j) + W(j) + Y(j-1) + Z(j)(X(j-1) + Y(j-1))$

After differential encoding, each of the two bits is applied to a separate trellis encoder (binary convolutional coder (BCC) with k = 5).
The following generating codes are employed:
G1 = 25 (octal) and G2 = 37 (octal).
Convolutional coding is followed by puncturing to a 4/5 code rate, i.e. the 2 x 4-bit BCC output data is converted to a serial data stream of 5-bit trellis groups.

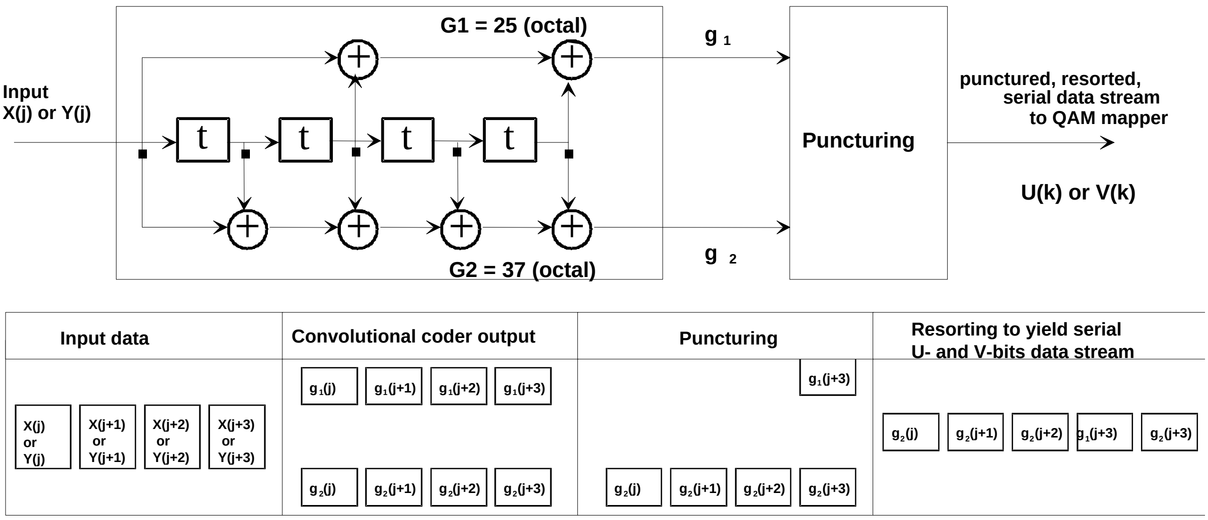

Fig. 5.14 Binary convolutional coder (BCC) and puncturing to code rate 4/5

All single function blocks of a 64QAM modulator with trellis coding have now been introduced.

Note the assignment of the uncoded "A" and "B" bits (MSBs) and the coded "U" and "V" bits (LSBs) to the C0 to C5 64QAM symbols in the overall block diagram:

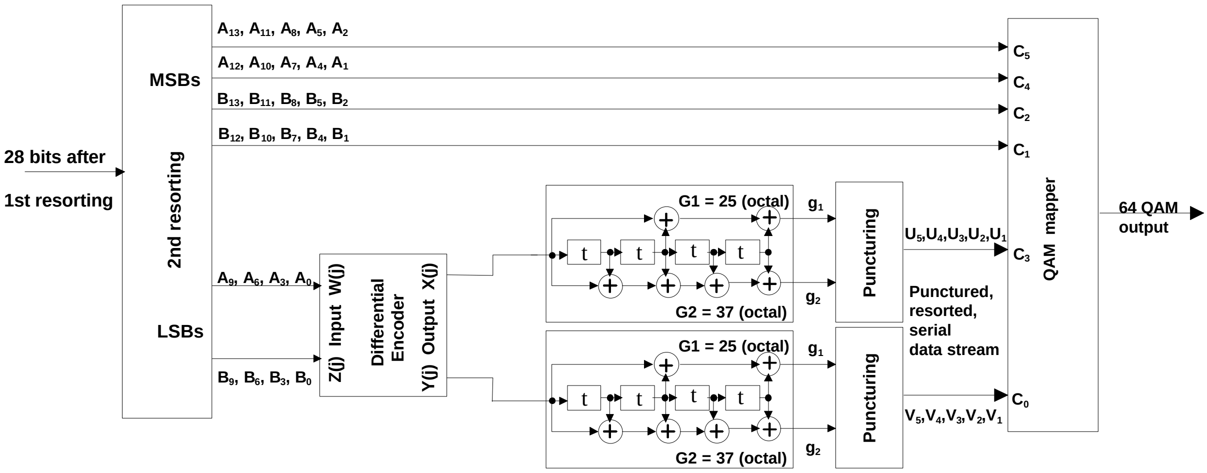

Fig. 5.15 64QAM modulator with trellis coding

The following overall code rate is obtained: 28/30 = 14/15

The 6-bit 64QAM symbols output by the QAM mapper are applied to the 64QAM modulator, which generates a constellation diagram with the 64QAM symbols mapped into bits as follows:

Q

110 111	111 011	010 111	011 011	100 101	101 111	110 101	111 111
110 100	111 000	010 100	011 000	100 000	101 010	100 000	111 010
100 111	101 011	000 111	001 011	000 101	001 111	010 101	011 111
100 100	101 000	000 100	001 000	000 000	001 010	010 000	011 010
010 011	011 001	000 011	001 001	000 001	001 101	100 001	101 101
010 110	011 100	000 110	001 100	000 010	001 110	100 010	101 110
110 011	111 001	100 011	101 001	010 001	011 101	110 001	111 101
110 110	111 100	100 110	101 100	010 010	011 110	110 010	111 110

$C_5C_4C_3\ C_2C_1C_0$

I

Fig. 5.16 64QAM constellation diagram for ITU-T J.83/B standard

The 64QAM symbols are $\sqrt{\cos}$ roll-off filtered analog pulses with a spectrum approximating a sin (x)/x function and eight amplitude levels for the I and the Q component. The eight amplitudes are represented by three bits each for I and Q.

Each symbol consists of a pair of I and Q values arranged orthogonally through modulation. 'I' stands for the in-phase and 'Q' for the quadrature component.
The resulting signals, therefore, have a defined flat spectrum (see Fig. 5.1 on the right).

5.1.6.2 Mapping of Randomized Data to 256QAM Symbols

For 256QAM, there are two types of trellis groups referred to as 'non-sync' and 'sync'. A non-sync trellis group consists of 38 data bits, a sync group of 30 data bits and 8 sync bits. Since each RS FEC frame comprises 88 RS blocks plus the 40-bit frame sync trailer, 2076 trellis groups per frame are obtained. The first 2071 trellis groups carry data bits only; the last 5 trellis groups carry 30 data bits and 8 sync bits each. The bits of the trellis groups are resorted and organized in 'A' symbols and 'B' symbols as shown in Fig. 5.17.

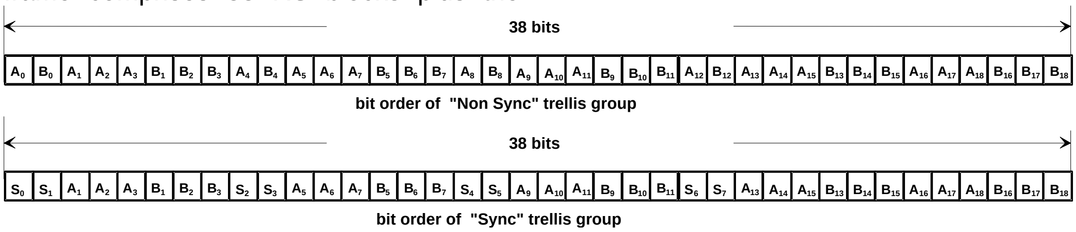

Fig. 5.17. 'A', 'B' and 'S' bits of 256QAM trellis groups

The trellis groups thus obtained are applied to the input of the 256QAM trellis coded modulator. In the input block of the 256QAM modulator, the 'A', 'B' and 'S' bits are resorted a second time, and the six MSBs and the two LSBs for the QAM mapper are generated. The six MSBs are input to the mapper uncoded, the two LSBs undergo differential encoding.

The data has the following structure:

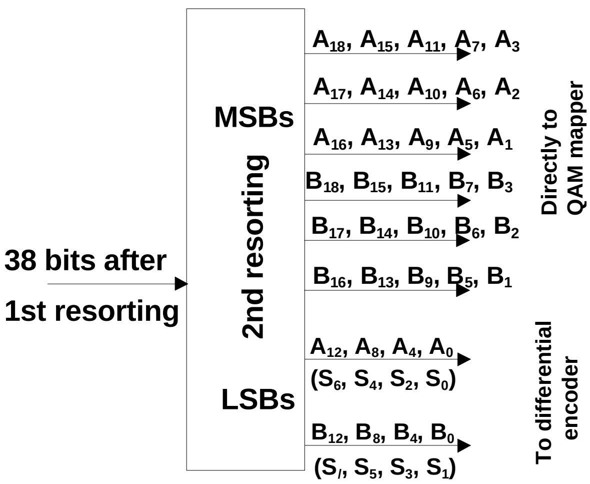

Fig. 5.18 Second resorting of bits of trellis groups

Tabular representation of trellis group symbols after second resorting:

	256QAM symbols of non-sync trellis group				
	T_0	T_1	T_2	T_3	T_4
Directly to mapper	B_3	B_7	B_{11}	B_{15}	B_{18}
	B_2	B_6	B_{10}	B_{14}	B_{17}
	B_1	B_5	B_9	B_{13}	B_{16}
	A_3	A_7	A_{11}	A_{15}	A_{18}
	A_2	A_6	A_{10}	A_{14}	A_{17}
	A_1	A_5	A_9	A_{13}	A_{16}
To diff. encoder	B_0	B_4	B_8	B_{12}	
	A_0	A_4	A_8	A_{12}	

Table 5.4 256QAM symbols of non-sync trellis group

	256QAM symbols of sync trellis group				
	T_0	T_1	T_2	T_3	T_4
Directly to mapper	B_3	B_7	B_{11}	B_{15}	B_{18}
	B_2	B_6	B_{10}	B_{14}	B_{17}
	B_1	B_5	B_9	B_{13}	B_{16}
	A_3	A_7	A_{11}	A_{15}	A_{18}
	A_2	A_6	A_{10}	A_{14}	A_{17}
	A_1	A_5	A_9	A_{13}	A_{16}
To diff. encoder	S_1	S_3	S_5	S_7	
	S_0	S_2	S_4	S_6	

Table 5.5 256QAM symbols of sync trellis group

Table 5.3 shows that symbol T_4 has only six bits. The remaining two bits are generated by the trellis encoder and subsequent puncturing.
The above tables also show that the data of a trellis group corresponds to the five 8-bit 256QAM symbols T_0, T_1, T_2, T_3 and T_4.

Before being applied to the trellis encoder, the two LSBs undergo differential encoding, which considerably enhances decoding reliability of the ITU-T J.83/B receiver.

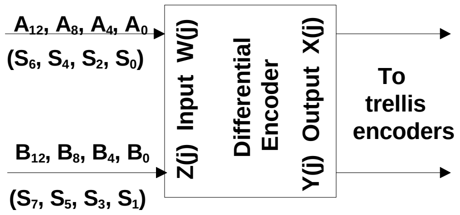

Fig. 5.19 Differential encoder

Differential encoding is based on the following equations:

X(j) = W(j) + X(j-1) + Z(j)(X(j-1) + Y(j-1)) and
Y(j) = Z(j) + W(j) + Y(j-1) + Z(j)(X(j-1) + Y(j-1))

After differential encoding, each of the two bits is applied to a separate trellis encoder (binary convolutional coder (BCC) with k = 5).

The following generating codes are employed:
G1 = 25 (octal) and G2 = 37 (octal)

Convolutional coding is followed by puncturing to a 4/5 code rate, i.e. the 2 x 4-bit BCC output data is converted to a serial data stream of 5-bit trellis groups.

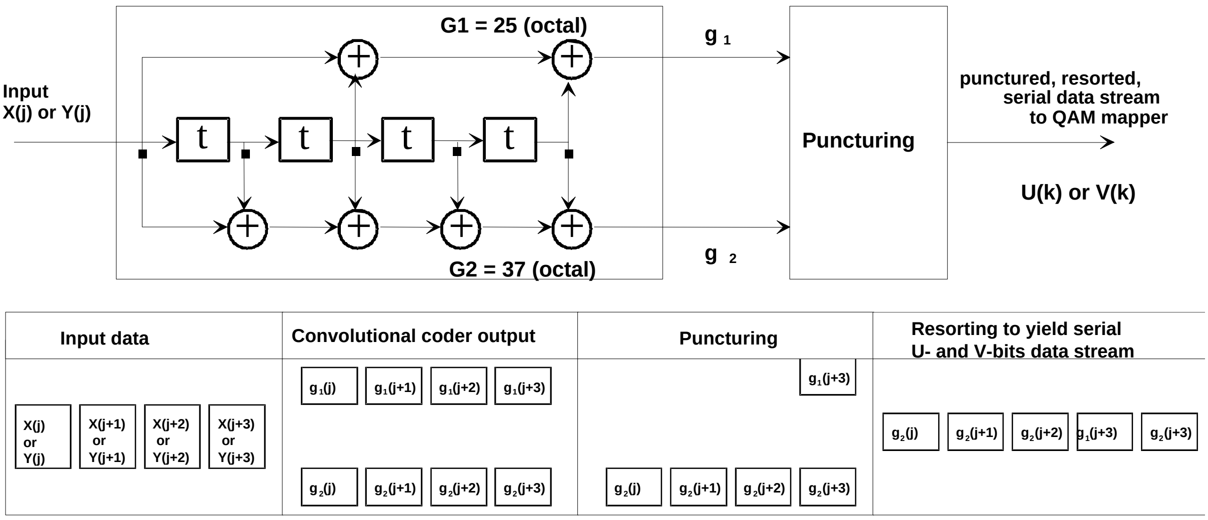

Fig. 5.20 Binary convolutional coder (BCC) and puncturing to code rate 4/5

All single function blocks of the 256QAM modulator with trellis coding have now been introduced.

Note the assignment of the uncoded "A" and "B" bits (MSBs) and the coded "U" and "V" bits (LSBs) to the C0 to C7 256QAM symbols in the overall block diagram:

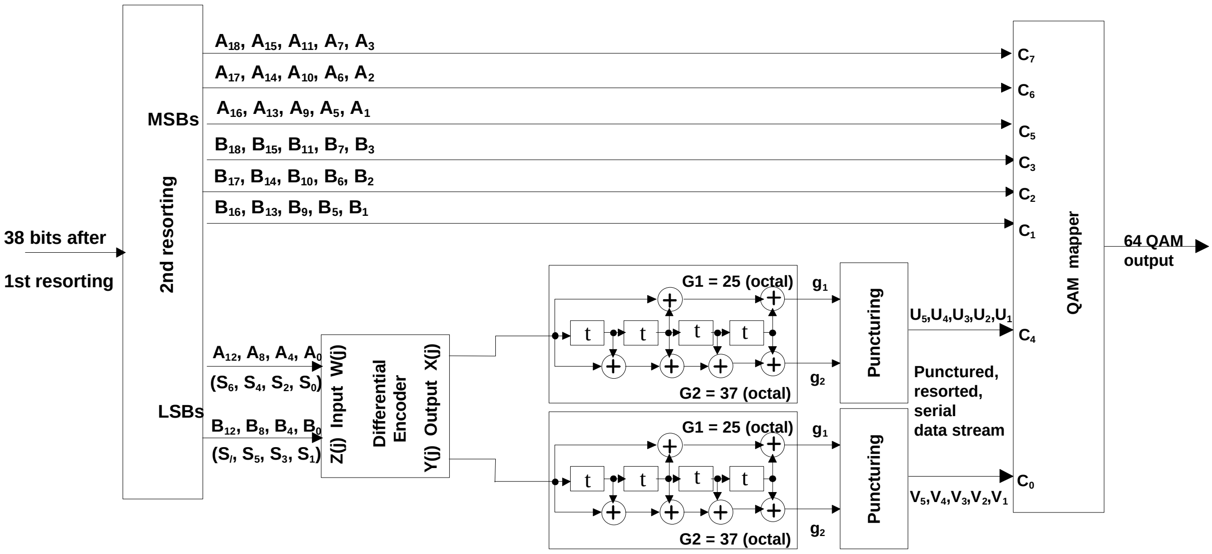

Fig. 5.21 256QAM modulator with trellis coding

The following overall code rate is obtained: 38/40 = 19/20

The 8-bit 256QAM symbols output by the QAM mapper are applied to the 256QAM modulator, which generates a constellation diagram with the 256QAM symbols mapped into bits as follows:

Q

1110 1111	1111 1101	1110 1011	1111 1001	1110 0111	1111 0101	1110 0011	1111 0001	0000 1111	0011 1111	0100 1111	0111 1111	1000 1111	1011 1111	1100 1111	1111 1111
1100 1110	1101 1100	1100 1010	1101 1000	1100 0110	1101 0100	1100 0010	1101 0000	0000 1100	0011 1100	0100 1100	0111 1100	1000 1100	1011 1100	1100 1100	1111 1100
1010 1111	1011 1101	1010 1011	1011 1001	1010 0111	1011 0101	1010 0011	1011 0001	0000 1011	0011 1011	0100 1011	0111 1011	1000 1011	1011 1011	1100 1011	1111 1011
1000 1110	1001 1100	1000 1010	1001 1000	1000 0110	1001 0100	1000 0010	1001 0000	0000 1000	0011 1000	0100 1000	0111 1000	1000 1000	1011 1000	1100 1000	1111 1000
0110 1111	0111 1101	0110 1011	0111 1001	0110 0111	0111 0101	0110 0011	0111 0001	0000 0111	0011 0111	0100 0111	0111 0111	1000 0111	1011 0111	1100 0111	1111 0111
0100 1110	0101 1100	0100 1010	0101 1000	0100 0110	0101 0100	0100 0010	0101 0000	0000 0100	0011 0100	0100 0100	0111 0100	1000 0100	1011 0100	1100 0100	1111 0100
0010 1111	0011 1101	0010 1011	0011 1001	0010 0111	0011 0101	0010 0011	0011 0001	0000 0011	0011 0011	0100 0011	0111 0011	1000 0011	1011 0011	1100 0011	1111 0011
0000 1110	0001 1100	0000 1010	0001 1000	0000 0110	0001 0100	0000 0010	0001 0000	0000 0000	0011 0000	0100 0000	0111 0000	1000 0000	1011 0000	1100 0000	1111 0000
1110 0001	1101 0001	1010 0001	1001 0001	0110 0001	0101 0001	0010 0001	0001 0001	0000 0001	0001 0011	0000 0101	0001 0111	0000 1001	0001 1011	0000 1101	0001 1111
1110 0010	1101 0010	1010 0010	1001 0010	0110 0010	0101 0010	0010 0010	0001 0010	0010 0000	0011 0010	0010 0100	0011 0110	0010 1000	0011 1010	0010 1100	0011 1110
1110 0101	1101 0101	1010 0101	1001 0101	0110 0101	0101 0101	0010 0101	0001 0101	0100 0001	0101 0011	0100 0101	0101 0111	0100 1001	0101 1011	0100 1101	0101 1111
1110 0110	1101 0110	1010 0110	1001 0110	0110 0110	0101 0110	0010 0110	0001 0110	0110 0000	0111 0010	0110 0100	0111 0110	0110 1000	0111 1010	0110 1100	0111 1110
1110 1001	1101 1001	1010 1001	1001 1001	0110 1001	0101 1001	0010 1001	0001 1001	1000 0001	1001 0011	1000 0101	1001 0111	1000 1001	1001 1011	1000 1101	1001 1111
1110 1010	1101 1010	1010 1010	1001 1010	0110 1010	0101 1010	0010 1010	0001 1010	1010 0000	1011 0010	1010 0100	1011 0110	1010 1000	1011 1010	1010 1100	1011 1110
1110 1101	1101 1101	1010 1101	1001 1101	0110 1101	0101 1101	0010 1101	0001 1101	1100 0001	1101 0011	1100 0101	1101 0111	1100 1001	1101 1011	1100 1101	1101 1111
1110 1110	1101 1110	1010 1110	1001 1110	0110 1110	0101 1110	0010 1110	0001 1110	1110 0000	1111 0010	1110 0100	1111 0110	1110 1000	1111 1010	1110 1100	1111 1110

I

$C_7C_6C_5C_4$
$C_3C_2C_1C_0$

Fig. 5.22 256QAM constellation diagram for ITU-T J.83/B standard

The 256QAM symbols are $\sqrt{\cos}$ roll-off filtered analog pulses with a spectrum approximating a sin (x)/x function and 16 amplitude levels for the I and the Q component. The 16 amplitudes are represented by four bits each for I and Q.

Each symbol consists of a pair of I and Q values arranged orthogonally through modulation. 'I' stands for the in-phase and 'Q' for the quadrature component.
The resulting signals, therefore, have a defined flat spectrum (see Fig. 5.1 on the right).

5.2 64QAM and 256QAM Signal Bandwidths

5.2.1 64QAM Signal Bandwidth

The bandwidth is determined based on the specified R_{N64} net data rate for 64QAM, which is 26.97035 Mbit/s. From the net data rate, the gross data rate is calculated as follows:

$$R_{G64} = R_{N64} * \frac{((122+6)*7*60)+42}{122*7*60} * \frac{15}{14} \text{ Mbit/s}$$

$$= 30.34164375 \text{ Mbit/s}$$

Each 64QAM symbol takes up 6 bits of the R_{G64} gross data rate. From this, the symbol rate S is obtained which, expressed in Hz, constitutes the signal bandwidth:

$$BW_{64} = \frac{30.34164375}{6} = 5.056940625 \text{ MHz}$$

The M/NTSC channel bandwidth is

$$BW_{Channel} = 6 \text{ MHz}$$

Based on the signal bandwidth

$$BW_{64} = 5.056940625 \text{ MHz}$$

the optimal roll-off factor r is calculated as follows:

$$r = 1 - \frac{BW_{Channel}}{BW_{64}} = 1 - \frac{6.0}{5.056940625} = 0.186488$$

which is 18.6488 % expressed in percent. The ITU-T J.83/B standard defines an 18 % roll-off factor for 64QAM.

5.2.2 256QAM Signal Bandwidth

The bandwidth is determined based on the specified net data rate R_{N256} for 256QAM, which is 38.81070 Mbit/s. From the net data rate, the gross data rate is calculated as follows:

$$R_{G256} = R_{N256} * \frac{((122+6)*7*88)+40}{122*7*88} * \frac{20}{19} \text{ Mbit/s}$$

$$= 42.884294869 \text{ Mbit/s}$$

Each 256QAM symbol takes up 8 bits of the R_{G256} gross data rate. From this, the symbol rate S is obtained which, expressed in Hz, constitutes the signal bandwidth:

$$BW_{256} = \frac{42.884294869}{8} = 5{,}360536858625 \text{ MHz}$$

The M/NTSC channel bandwidth is

$$BW_{Channel} = 6 \text{ MHz}$$

Based on the signal bandwidth

$$BW_{256} = 5.360536858625 \text{ MHz}$$

the optimal roll-off factor r is calculated as follows:

$$r = 1 - \frac{BW_{Channel}}{BW_{256}} = 1 - \frac{6.0}{5.360536858625} = 0.119291$$

which is 11.9291 % expressed in percent. The ITU-T J.83/B standard defines a 12 % roll-off factor for 256QAM.

5.2.3 $\sqrt{\cos}$ Filtering at Transmitter and Receiver End

The symbols shaped by $\sqrt{\cos}$ filters in the transmitter and the receiver yield a spectrum similar to a sin x/x function with a constant amplitude- and group-delay frequency response. $\sqrt{\cos}$ filtering in the transmitter and the receiver produces spectrum edges as shown in Fig. 5.24 "Spectrum obtained by cos roll-off filtering". The degree of approximation to an ideal sinx/x spectrum depends on the selected roll-off factor. The smaller this factor, the better the approximation to an ideal sinx/x spectrum.
Plotting the level along a linear scale, the following theoretical spectrum will be obtained at the output of an ITU-T J.83/B modulator:

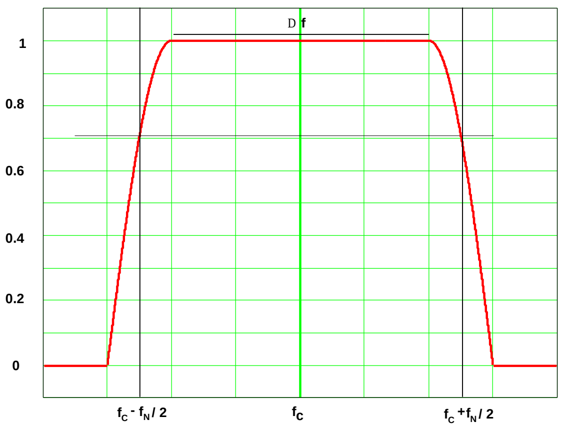

Fig. 5.23 Spectrum obtained by $\sqrt{\cos}$ filtering
Clearly discernible are the steep edges at low levels at the left and right boundaries of the

spectrum produced by $\sqrt{\cos}$ filtering. Attenuation at the Nyquist frequencies $f_C \pm f_N /2$ is 3 dB.

The roll-off factor r is based on the ratio of the Nyquist bandwidth to the flat "rooftop" of the spectrum:

$$r = \frac{f_N}{\Delta f} - 1$$

$\sqrt{\cos}$ filtering in the transmitter and the receiver yields spectrum edges with a cos roll-off characteristic.

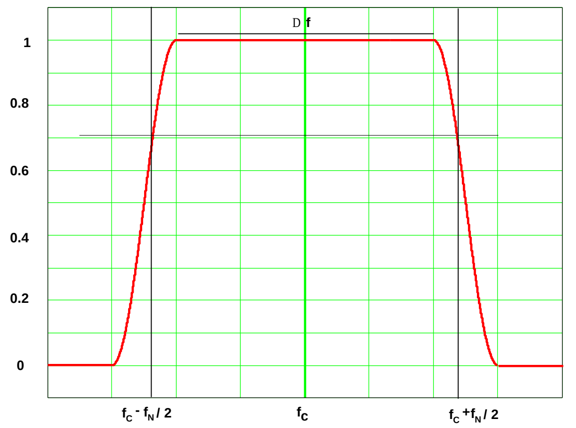

Fig. 5.24 Spectrum obtained by cos roll-off filtering

It can be seen that with cos filtering the edges at low levels at the left and right boundaries of the spectrum are flatter and rounder. Attenuation at the Nyquist frequencies $f_C \pm f_N /2$ is now 6 dB.

To illustrate this, Fig. 5.25 shows the $\sqrt{\cos}$ and cos filter edges in greater detail:

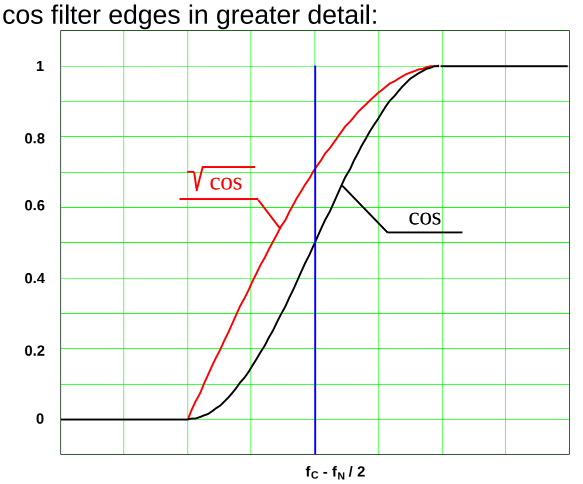

Fig. 5.25 Edges obtained with $\sqrt{\cos}$ roll-off and cos roll-off filtering

Combined filtering in the transmitter and the receiver serves three purposes:

1. The Nyquist criterion is fully met, so the transmitted signal can be retrieved accurately and error-free at the receiver end.
2. In case of noisy transmissions, combined transmitter and receiver $\sqrt{\cos}$ filtering enables optimal noise filtering in the receiver.
3. By signal filtering in the receiver, useful channel selection is effected at the same time.

The required bandwidth for the transmission channel (B_{Ch}) is derived from the symbol rate S and the roll-off factor r as follows:

$$BW_{Ch} = S*(1+r)\ \text{MHz}$$

5.3 ITU-T J.83/B Key Data

QAM mode	64 256	
Symbol form		Similar to $\frac{\sin x}{x}$ cos roll-off filtered
Roll-off factor	64QAM 256QAM	0.18 0.12
Net bit rate R (Mbit/s)	64QAM 256QAM	26.97035 38.81070
Gross bit rate R (Mbit/s)	64QAM 256QAM	30.34164375 42.884294869
Symbol rate S (Msymb/s)	64QAM 256QAM	5.056940625 5.360536858625

Table 5.6

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5.3 Data Rates and Symbol Rates in ITU-T J.83/B

An MPEG2 multiplexer or an MPEG2 generator supplies video, audio and other data in the form of TS (transport stream) packets with a defined data rate R. ITU-T J.83/B specifies two gross data rates:

Gross data rate for 64QAM:

R_{G64} = 30.34164375 Mbit/s

Gross data rate for 256QAM:

R_{G256} = 42.884294869 Mbit/s

Each symbol carries
6 bits for 64QAM or
8 bits for 256QAM
of the MPEG2 data stream, i.e. three or four bits each for the I and the Q component.

This yields the following symbol rates:

S_{64} = 5.056940625 Msymb/s
S_{256} = 5.360536859 Msymb/s

The above data rates and symbol rates must be accurately complied with. Deviations > $1 * 10^{-5}$ might cause signal processing in the transmitter and, even more critically, in the receiver to fail, since the quartz PLLs reach the limits of their pull-in range. Monitoring and measuring the data and symbol rates is therefore a must.

The data rates specified by ITU-T J.83/B for 64QAM and 256QAM can be changed on the Rohde & Schwarz TV Test Transmitters R&S SFQ and R&S SFL-J by changing the symbol rate as follows:

For 64QAM:
between 4.5 Msymb/s and 5.625 Msymb/s (corresponding to a variation of the gross data rate between 27.0 Mbit/s and 33.75 Mbit/s)

For 256QAM:
between 4.8 Msymb/s and 5.9 Msymb/s (corresponding to a variation of the gross data rate between 38.4 Mbit/s and 47.2 Mbit/s).

The pull-in range of the symbol rate PLL of set-top boxes (STBs) for the American ITU-T J.83/B cable standard can thus easily be monitored.

The setting range for the symbol rate is in either case much larger than the actual pull-in range of the STB's PLL.

For measurements to the ITU-T J.83/B digital television (DTV) standard, the R&S SFQ and the R&S SFL-J modulate the TS data stream strictly in accordance with specifications. In addition, defined modulation errors can be introduced into the ideal signal, for example a symbol rate deviating from the ideal value, and thus reproducible signal degradation created. Such stress signals are indispensable in DTV receiver tests to determine the system limits.